Amendments to the Specification:

Please replace paragraph **[0015], [0016], [0063], [0067],** and **[0083]** with the following amended paragraphs:

[0015] ~~Figure 6 illustrates an example~~ Figures 6A and 6B illustrate examples of ~~a~~ bit shifter ~~circuit~~ circuits with five multiplexers according to ~~an embodiment~~ embodiments of the present invention;

[0016] Figure 7 illustrates an example of the multiplexers that can be used with the bit shifter ~~circuit of Figure 6~~ circuits of Figures 6A and 6B according to an embodiment of the present invention;

[0063] Bit shifter circuits 501-503 receive the five output voltages [V_{B4}, V_{B3}, V_{B2}, V_{B1}, V_{B0}] from digital encoder circuit 104. Voltages V_{B4}, V_{B3}, V_{B2}, V_{B1}, and V_{B0} are referred to as BIT4, BIT3, BIT2, BIT1, and BIT0, respectively, in Figure **[[6]]** 6A. Circuits 501-503 can shift bits BIT0-BIT4 to the right or to the left in response to the state of RAM bits stored in RAM cells 511-513, respectively.

[0067] Figure **[[6]]** 6A illustrates an example of circuitry 600 that can be used to implement each of bit shifters 501-503. Circuit 600 includes multiplexers 601-605. In general circuit 600 has the same number of multiplexers as there are bits generated by encoder 104. Thus, if encoder 104 generates a four bit signal, then circuit 600 has four multiplexers.

[0083] According to further embodiments, a bit shifter circuit of the present invention can shift bits BIT4-BIT0 to the left or to the right by two or more bits to increase/decrease the on-chip termination impedance by a larger amount. In an embodiment that can shift left or right by two bits, each multiplexer in the bit shifter circuit has five input terminals, four of which are coupled to adjacent bit signals or ground. A 2-bit shifter allows a user to match 0.25R. 0.5R, R, 2R, and 4R, where R is the matching resistance when the bit shifter does not shift any of the bits. An example of one such bit shifter circuit is shown in Figure 6B.